**IN THE CLAIMS**

This listing of claims will replace all prior versions and listings of claims in the application:

**LISTING OF CLAIMS:**

1. (Amended) A method for fabricating a gate electrode of a semiconductor device, comprising the steps of:

forming a gate insulation layer on a substrate;

forming a gate layer structure containing at least a metal layer on the gate insulation layer;

forming a hard mask oxide layer on the gate layer structure at a temperature lower than an oxidation temperature of the metal layer, wherein the hard mask oxide layer is obtained by performing an atomic layer deposition (ALD) technique at a temperature ranging from about 70 °C to about 350 °C;

forming a hard mask nitride layer on the hard mask oxide layer;

patterning the hard mask oxide layer and the hard mask nitride layer as a double hard mask for forming the gate electrode; and

forming the gate electrode by etching the gate layer structure with use of the double hard mask as an etch mask.

2. (Canceled)

3. (Original) The method as recited in claim 1, wherein the step of forming the hard mask oxide layer includes the step of performing an annealing process for densifying the hard mask oxide layer and removing remnant impurities.

4. (Original) The method as recited in claim 3, wherein the annealing process is performed at a temperature ranging from about 400 °C to about 1000 °C in an atmosphere of $N_2$ gas, $H_2$ gas or a mixed gas of $N_2$ and $H_2$ for about 10 seconds to about 30 minutes.

5. (Original) The method as recited in claim 1, wherein the hard mask oxide layer is made of a material selected from a group consisting of $SiO_2$, $SiO_xN_y$, where x and y representing atomic ratios of oxygen and nitrogen range from about 0 to about 2.0 and from about 0 to about 1.0, respectively and $SiO_xF_y$, where x and y representing atomic ratios of oxygen and fluorine range from about 0 to about 2.0 and from about 0 to about 1.0, respectively or a group consisting of $HfO_2$, $ZrO_2$, $Ta_2O_5$, $Al_2O_3$, $La_2O_3$, $Y_2O_3$ and $CeO_2$.

6. (Original) The method as recited in claim 1, wherein the hard mask oxide layer has a thickness ranging from about 10 Å to about 1000 Å.

7. (Original) The method as recited in claim 1, wherein the gate layer structure is a structure selected from a stack structure of a metal layer, a diffusion barrier layer and a polysilicon layer, a stack structure of a silicide layer and a polysilicon layer, a stack structure of a metal layer, a diffusion barrier layer and a polysilicon-germanium layer and a single metal structure containing only a metal layer.

8. (Original) A method for fabricating a gate electrode of a semiconductor device, comprising the steps of:

forming a gate insulation layer on a substrate;

forming a gate layer structure including at least a metal layer on the gate insulation layer;

forming a hard mask oxide layer on the gate layer structure at a temperature lower than an oxidation temperature of the metal layer;

forming a triple hard mask by stacking a hard mask nitride layer and a hard mask conductive layer on the hard mask oxide layer;

patterning the triple hard mask to be used for forming the gate electrode; and

forming the gate electrode by etching the gate layer structure with use of the patterned triple hard mask as an etch mask.

9. (Original) The method as recited in claim 8, wherein the step of forming the hard mask oxide layer proceeds by performing an ALD technique at a temperature ranging from about 70 °C to about 350 °C.

10. (Original) The method as recited in claim 8, wherein the step of forming the hard mask oxide layer includes the step of performing an annealing process for densifying the hard mask oxide layer and removing remnant impurities.

11. (Original) The method as recited in claim 10, wherein the step of performing the annealing process is performed at a temperature ranging from about 400 °C to about 1000 °C in an atmosphere of $N_2$ gas, $H_2$ gas or a mixed gas of $N_2$ and $H_2$ for about 10 seconds to about 30 minutes.

12. (Original) The method as recited in claim 8, wherein the hard mask oxide layer is made of a material selected from a group consisting of $SiO_2$, $SiO_xN_y$, where x and y representing atomic ratios of oxygen and nitrogen range from about 0 to about 2.0 and from about 0 to about 1.0, respectively and $SiO_xF_y$, where x and y representing atomic ratios of oxygen and fluorine range from about 0 to about 2.0 and from about 0 to about 1.0, respectively or a group consisting of $HfO_2$, $ZrO_2$, $Ta_2O_5$, $Al_2O_3$, $La_2O_3$, $Y_2O_3$ and $CeO_2$.

13. (Original) The method as recited in claim 8, wherein the hard mask oxide layer has a thickness ranging from about 10 Å to about 1000 Å.

14. (Original) The method as recited in claim 8, wherein the gate layer structure is a structure selected from a stack structure of a metal layer, a diffusion barrier layer and a polysilicon layer, a stack structure of a silicide layer and a polysilicon layer, a stack structure of a metal layer, a diffusion barrier layer and a polysilicon-germanium layer, a stack structure of a silicide layer and a polysilicon germanium layer and a single metal structure containing only a metal layer.

15. (Original) The method as recited in claim 8, wherein the hard mask conductive layer is a tungsten layer or a tungsten nitride layer.